TITLE OF THE INVENTION

TIMING CONTROL MEANS FOR AUTOMATIC COMPENSATION OF TIMING UNCERTAINTIES

5   CROSS-REFERENCES TO RELATED APPLICATIONS

This application is a Continuation-in-Part of a PCT application PCT/RU01/00 filed on 22 May 2001 claiming priorities of PCT/RU00/00188 filed on 22 May 2000 and US Provisional application 60/228,115 filed on 28 August 2000.

10   STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OF DEVELOPMENT

Not applicable.

BACKGROUND OF THE INVENTION

15   1. Field of the invention

The present invention relates to the reducing of timing uncertainties in high-performance multiple channel devices. More specifically, the present invention relates to a device and method for minimizing timing uncertainties due to asymmetry of rising and falling edges and also duty cycle inaccuracy. The

20   invention can be employed in a digital interface between two items or within a circuit where there is a requirement for tight timing control such as requirement for a low skew between the channels of a register.

The present invention is particularly applicable to digital systems of data transmission, interfaces to memory devices, to test equipment for testing

25   semiconductor devices and to high-speed communications, especially for systems with double data transmission rate (DDR).

2. Description of the Related Art Including Information Disclosed Under 37 CFR 1.97 and 1.98

Transistor linewidths have been reducing according to Moore's Law since around 1971: this involves a doubling of the density of transistors every 18 months. The speed of a transistor, such as a MOSFET, is proportional to the inverse of the square of the channel length, which means that many integrated circuits are now able to operate at speeds above 1GHz internally. Except for a small number of extremely complicated interfaces, or for serial interfaces, the interface speeds have been a small fraction of the maximum chip operating speed. Another problem has been the width of the interface: the problem of skew between signal lines has hitherto prevented wide interfaces from operating at high frequency, hence creating a fundamental limit to the bandwidth than an interface can carry.

In another example, that of Automatic Test Equipment (ATE), a substantial complexity of deskew circuitry has been required to test high speed devices. Moreover, as soon as the device is under test, the heat generated by the environment of the drivers, the drivers themselves and other factors has caused the skew to alter during the test.

Known is the use of analogue increments to automatically self-calibrate a pulse generator described in US 5,430,660. During the calibration, the output of the oscillator is used to produce output pulses whose edge locations are then adjusted by small digital increments or "slivers" and very small analogue increments or "verniers". The RAM contents are converted to a serial bit stream that controls the coarse pulse width and period as an integral number of top octave periods, or quanta. However, this method of skew control is not automatic and requires an operator to disconnect the generator from the working circuit and connect an output of the generator to a calibration input in order to accomplish the calibration.

It has been a growing tendency in high speed communications, in particular, digital systems of data transmission, to increase data transmission rates and timing accuracy. However, as frequency grows, a problem arises of accurate and reliable reading of previous and subsequent symbols by various devices for receiving and transmitting data.

For digital circuit devices such as flip-flops, latches and other storage circuits, accurate reading of signals is possible only provided strict requirements to set-up and hold times are observed, where "set-up time" is the time before the clock edge during which data are required to be present and stable, and "hold time" is the time after the clock edge during which data are required to be present and stable. These requirements result in that the maximum clock frequency is limited by the sum of hold and set-up times; therefore, it is desirable that set-up and hold time be as short as possible.

Different attempts have been made to improve setup and hold time characteristics, however, a thorough analysis of component elements of setup/hold times is absent in the available art, therefore, it would be helpful to gain a better understanding of phenomena taking place at that.

In Fig.7a, a block scheme of a real flip-flop is presented, which consists of an ideal flip-flop FF which is noiseless, hysteresis-free and has zero setup and hold times. A real flip-flop additionally comprises delays Td and Tc in data and clock paths, respectively. Also, there is a source N of phase noise in clock path and a source of hysteresis H.

The delays Td and Tc depend on such parameters as temperature, supply voltage, direction of transition (rising or falling edge), frequency of signal and others. The combination of Td and Tc gives a value of setup/hold time which provides stable data transmission. For example, assuming Td varies from 0 to 1ns, Tc varies from 0 to 1ns, each independently, it would be impossible to read data earlier than 1ns after the change occurs, with respect to clock, or less than 1ns before the change that gives the values of setup time = 1ns, hold time = 1ns.

Furthermore, phase noise extends setup and hold times for the value of phase noise.

Flip-flops are often used to synchronize signals operating at different frequencies to a local clock. However, since the signals are asynchronous to the local clock, the setup and hold time specifications associated with the flip-flop are sure to be violated. When the setup and hold time is violated, the output response of the flip-flop is uncertain. The output may assume a "metastable" state, defined as the time period during which the output of a digital logic device is not at logic level 1 or logic level 0, but instead resides at an output level between logic level 0 and logic level 1. The voltage ranges corresponding to different logic levels are specified by the manufacturer of the device. For bipolar TTL technology, for example, the metastable region might lie between 0.8 volts and 2.0 volts.

The metastable problem occurs when the signal being input to the flip-flop is undergoing a transition from one logic level to the other simultaneously with the active edge of the local clock pulse, causing the latch section of the flip-flop to latch at the intermediate voltage level. Since the input data is changing while it is being clocked, the system designer does not care if the flip-flop goes to either a high or low logic level in this instance, just so long as the output does not "hang-up" in the metastable region. Eventually, the output of the flip-flop will stabilize at a valid logic level; however, logic circuitry following the flip-flop depends upon the delay specification (stated time period from the clock pulse to a valid output) being met. A metastable output may cause this logic circuitry to fail. Thus, the metastable characteristics of the flip-flop used to synchronize an asynchronous data stream can influence overall system reliability.

One approach to mitigate the problem of metastable outputs is to provide a second flip-flop in series with the first flip-flop, or more flip-flops cascaded as proposed in US 4,929,850. The clock to the second flip-flop is delayed relative to clock to the first flip-flop, thus allowing time for the output signal of the first flip-flop to stabilize at a valid logic level before clocking the data into the second flip-

flop. In many applications, this delay is excessive. Furthermore, the logic may still fail if the output of the first flip-flop remains in the metastable region for a period greater than the delay between the clocks.

Thus, the traditional solution of employing two serially connected flip flops
5   is not desirable in applications where an output is needed rapidly. The use of the second flip flop delays the resulting output by an entire clock period. In order to rapidly provide this output, it has also been proposed to rapidly resolve internal logic signals through the use of the deselect synchronizer, instead of two flip flops.

10   Another approach is described in US 6,002,282 according to which a closed-loop clock delay adjustment system compensates the difference between the delay introduced by on-chip clock buffers and delays inserted at the device data input pins. By measuring the actual real time drift, the clock buffer delay is adjusted to minimise the input set-up time without additional requirements to hold
15   time. The value of Tc is adjusted at a rising edge with the same value of Td that provides a significant reduction in setup/hold time.

However, even after the adjustment is made, there are still phase noise and asymmetry of the rising and falling edges that influence the setup/hold time.

Moreover, the moment of reading data depends also on frequency
20   because the system described in US 6,002,282 uses as a reference an internal clock of high frequency which is inaccurate to the extent it is frequency dependent, because a high frequency clock has additional frequency-dependent phase errors due to system parasitics.

One more source of errors is the hysteresis at the receiver which
25   increases setup/hold time for the value of hysteresis. However, still the most important phenomena that has not been taken into consideration until now, but yet influencing the accuracy of operation of a digital device is that each flip-flop, latch and similar device can be defined by its inherent probability function of transition from "0" to "1" depending on set-up and hold times.

In Fig.10a is shown a sequence of symbols S1—Sn transmitted through a channel, where the former symbol S1 changes to the next symbol S2 at a moment "O".

Let us consider in more detail the moment of transition from signal S1 to signal S2 with reference to Fig.7c.

The probability of reading symbol S2 when the time is much less than "0" is equal to 0%, the same as the probability of reading symbol S2 at times much more than "0" is equal to 100%, while in time interval near 0, the probability changes smoothly from 0% to 100%, with value of 50% at time 0. This phenomenon is caused by system noise and other static errors and because of this, has a probabilistic nature.

It can be approximated by the following function:

$$P(t) = \frac{1+ \text{Erf}(t/\sigma)}{2}$$

where t - is the moment of reading data;

P - is the probability function;

σ - is rms (root-mean-square) value of phase noise.

An example probability function for a typical flip-flop is shown in Fig.7b, where P is the probability, and t is the time difference between the actual moment when the data is read and the moment when the data crosses a threshold of the flip-flop. It is possible to measure this probability function experimentally, e.g. using procedure described in details in WO 00/00837, published on 06.01.2000, the description of which is incorporated herein by reference.

For different moments of reading data, the probability of reading either new or previous data changes gradually from 0 to 100% of the time defined by the value of phase noise of the system in whole, so that a selected range of ΔP

would correspond to a predetermined level of timing uncertainty. It shall be mentioned that the term "timing uncertainty" relates to uncertainty of the moment of reading data caused by different reasons including phase noise, static input offset and others and reflects the total effect caused by a sum of these factors.

5 Thus, another term of high importance which is used within the context of the present invention and closely related to the uncertainty in reading data is "a probability of reading a desired symbol on a boundary of two symbols in a sequence of symbols transmitted through a channel". It is obvious from the figure, that if the placement of the moment when the data is read on the

10 probability function of transition from "0" to "1" is not controlled, no reliable data is obtained.

The above-described problems are exacerbated as timing tolerances become more severe with higher data transfer rates. For example, if the data clock does not latch the data applied at the proper time, data errors may result.

15 Similar problems exist in many memory devices, such as synchronous DRAMs, and contemporary microprocessors which must process control and other signals at a high rate of speed.

Unfortunately, there has heretofore been no suitable means for ensuring that digital signals are latched in high speed digital interfaces in proper time at

20 very high data transfer rates.

In PCT/RU00/00188 filed in the name of the applicant of the present invention, a timing control means is described for the compensation of timing errors in multiple channel devices wherein for each register a corresponding feedback loop is associated for the relative alignment of register's channels

25 timing in relation to the reference signal, said feedback loop comprising a means for detecting a deviation from a predetermined level of probability of reading by the register a desired symbol on a boundary of two reference channel symbols in a sequence to generate a feedback signal to compensate timing errors in said register.

By measuring real values of the probability function of transition from "0" to "1", according to PCT/RU00/00188, the actual moment of reading data may be determined with the accuracy equal to a very small fraction of the value of the phase noise causing this uncertainty that makes possible highly accurate (up to

5   subpicoseconds) placement of the average position of the moment of reading data.

However, the obtained accuracy is often insufficient when waveforms are asymmetrical with respect to the rising and falling edges. Another common problem for high speed data transmission is the inequity of duty cycles that is

10   especially sensible in DDR systems.

BRIEF SUMMARY OF THE INVENTION

The object of the invention is the provision of a high speed digital interface having multiple channels, in which digital signals are latched at the proper time at very high data transfer rates and that would be insensible to the asymmetry of

15   waveforms and inequity of duty cycles and other signal errors, as well as a system phase noise.

Thereby, an interface is provided involving drivers and receivers to have the minimum or predefined skew, regardless of whether that interface is within the same chip, within the same circuit board, or in different locations in the globe.

20   The advantages of the present invention is a great reduction in the cost and complexity of high speed interfaces, combined with an increase in the potential bandwidth. For example, the RAMBUS interface is essentially a serial interface straining the technology available to provide 9 to 18 bits of high speed parallel transfer. The present invention would involve no strain of technology, and

25   give a bandwidth which could be one or two orders of magnitude higher than the fastest RAMBUS components available today. At another level, an ATE system could reduce by an order of magnitude the cost of the skew control circuitry, which forms a very large part of the cost of a test head.

The invention concerns the control of timing within a register. The register

may have any number of outputs. For example, the invention enables any number of registers to have the same skew, which can even be controlled to be zero at all times during its operation.

In one aspect, the invention is a timing control means for the compensation of timing errors in multiple channel devices comprising at least one register, the means comprising a clock for providing a clock signal; a referencesignal generator for providing a reference signal applicable through a reference channel to the register for deskewing the register's channels; wherein for each said register a corresponding feedback loop is associated for the relative alignment of register's channels timing in relation to the reference signal, said feedback loop comprising a means for detecting a deviation from a predetermined level of probabilityof reading by the register a desired symbol on a boundary of two reference channel symbols in a sequence and a set of delay means which uses the determined information on deviation from the fixed level of this probability to generate a feedback signal to compensate timing errors in said register.

The invention uses a channel of the register to take a reference signal which is offset in phase from the register's clock. For example it can be the clock signal delayed by a stable structure such as a pcb track. The output of the register taking this reference channel is applied to an integrator which implements the detecting means to create a negative feedback signal which is applied to a delay circuit with a monotonic transfer function on the clock input to the register.

In the diagram of Fig.10c, which is called an eye diagram, an interval of timing uncertainty is shown with respect to the probability function of Fig.7b. Increases in phase offset between the sampling point and the transition of the reference signal will create a pulse stream and the system will adapt to operate on a predetermined level of probability, which may be chosen as, e.g. the point where there is the maximum uncertainty, which means that 50% of the values are 0 and 50% are 1 in a binary digital system. This point is close to or the same as

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the point where metastability occurs and may include metastable phenomena in susceptible registers. For a description of metastability, refer to "Metastability and the ECLinPS™ Family" by Rennie Wm. Dover and Todd Pearson, AN1504, Motorola Inc., 1996; and also "High-Speed Digital Design: A Handbook of Black

5   Magic" by Howard W.Johnson and Martin Graham, Prentice Hall PTR, 1993, Englewood Cliffs, New Jersey 17632.

In another aspect of the invention, a self calibrating receiver comprises a register having a plurality of channels having inputs and outputs; a clock for providing a clock signal to the register; a reference signal generator connectable

10   to the input of at least one said channel of said register for supplying reference signals for deskewing the register; a detecting means connectable to the output of at least one said channel of said register for detecting a deviation from a predetermined level of probability of reading by said register a desired symbol on a boundary of two reference channel symbols in a sequence; wherein the output

15   of the detecting means is connectable to a set of delay means which uses the information received by said detecting means to generate a feedback signal to compensate timing errors in said register.

Where the register has a degree of hysteresis, this would produce a hunting effect whereby the skew varies around a mean. This hunting is typically

20   +/-45ps for registers using ALVCH technology – it appears to be a result of the use of a non-differential external clock which is passed through an inverter internally to the register, as well as other factors. To remove this skew variation, the reference signal can be modulated in phase to produce a feedback signal which extends in time to be wider than the width of the hysteresis. The integrator

25   will then have the effect within the feedback system of adjusting the clock phase to contain an equal number of 0s and 1s in a binary system, removing all hunting, without any detriment to the deskew accuracy.

In still another aspect of the invention, a self calibrating transmitter with expandable data width comprises at least one register having at least one

30   channel having an input and output; a clock means for providing a clock signal to

said register; a reference signal for supplying reference signals for deskewing said register's channel output in relation to the reference signal; a phase comparator, one input of which is connected to the reference signal and another input is connected to a sense signal at the register's output; and at least one

5   feedback loop associated with the output of said phase comparator, the feedback loop comprising a set of delay means to compensate the timing errors in transmitter channels, wherein the reference signal is connectable to the input of the phase comparator; and an input of at least one said channel of said register is connectable to another signal for providing the sense signal to the phase

10   comparator for deskewing the register.

It shall be mentioned that in this embodiment, the phase comparator serves as the detecting means for detecting a deviation from a predetermined level of probability of reading by said register a desired symbol on a boundary of two reference channel symbols in a sequence; wherein the information received

15   by said phase comparator is used to generate a feedback signal to compensate timing errors in said register.

Furthermore, the present invention provides also the means for enhancing the timing accuracy for high speed digital data transmission systems experiencing asymmetry of rising and falling edges as illustrated in Fig.8a, and/or

20   inequity of duty cycles as shown in Fig.8b. It shall be noted that rising edge in even data transmission slots and odd data transmission slots will be called even and odd rising edges, respectively, for the convenience of further explanation.

According to this aspect of the invention, the self-calibrating transmitter comprises the features as stated for the third embodiment, wherein said phase

25   comparator comprises at least one channel for providing rising edge sense signal and at least one channel for providing falling edge sense signal for deskewing the register, while the calibration is effected for even rising, even falling and odd rising edges.

Thus, a system using the present invention will have a skew not more than

the intra-register skew, which is caused for example by the parasitics of the device package and can be eliminated such as by compensatory track lengths in the printed circuit board (pcb) or by delays or verniers on each line or channel.

The above disclosed technique can be effectively applied for improving transmission parameters of high speed transmission systems including DDR systems, such as Rambus, or other systems in which the data rate is multiple of a main clock frequency.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

For a better understanding of the present invention and the advantages thereof and to show how the same may be carried into effect, reference will now be made, by way of example, without loss of generality, to the following description now taken in conjunction with the accompanying drawings in which:

Fig.1a shows a general block diagram of a timing control means according to the present invention.

Fig.1b shows wave forms for a Clock, Reference and Sample Enable signals generated in the system of Fig.1a.

Fig. 2a is a block diagram of a self calibrated receiver with a means for obviating the internal register's hysteresis using a modulator signal according to a second example embodiment of the present invention.

Fig.2b shows an example of an analog monotonic delay vernier which may be used as a variable delay 8 in Figs.1a and 2a.

Fig.2c is an example of a low pass filter 14 in Fig.2a.

Fig.2d is an example of an integrator 16 in Fig.2a.

Fig.3 is a detailed circuit diagram showing an example implementation of a source of modulator signal for obviating the internal register's hysteresis using the modulator signal generated from the same register.

Figs.4a-4c illustrate wave forms for a modulator signal (Fig.4a) which is in this case an output signal from integrator 26 and clock signal (Fig.4b) applicable to the system shown in Fig.3 according to the present invention and a resulting reference signal which is a superposition thereof (Fig.4c).

5   Figs.4d-4e show a DQ1 output signal from register 12 shown in Fig.3 in the absence of modulator signal (Fig.4d) and in the presence of modulator signal (Fig.4e).

Fig.4f shows a transfer function graph for monotonic delay vernier 28 and low pass filter 25 for a feedback loop shown in Fig.3.

10   Fig.5 is a block diagram of a self calibrated transmitter in accordance with a third example embodiment of the present invention.

Fig.6 is a block diagram of a self calibrated transmitter wherein an auxiliary self calibrated register is used to maintain output zero skew between multiple driving registers.

15   Fig.7a is a schematic representation of a non-ideal flip-flop.

Fig.7b shows an example probability function for a non-ideal flip-flop.

Fig.7c shows partially an "eye diagram" for a typical flip-flop. Fig.8a illustrates how the differences in wave forms for high and low voltage data cause timing inaccuracies.

20   Fig.8b shows wave forms for an initial clock signal (upper), a clock signal at the input of clock doubler corresponding to different values of control voltage at the input of duty cycle correction stage called threshold as shown in Fig.8c (middle) and a resulting doubled clock at the output of clock doubler (bottom).

Fig.8c is a block diagram of the duty cycle correction stage and clock 25   doubler according to the present invention.

Fig.9 is a block diagram of a self calibrated transmitter wherein one auxiliary self calibrated register is used for rising edge calibration on even cycles and another self calibrated register is used for falling edge calibration with

respect to reference and rising edge calibration on odd cycles. Fig.10a is a block diagram of a self calibrated transmission system comprising a driver and a receiver according to the present invention.

Fig.10b shows wave forms for a clock and reference signals provided in
5   the system of Fig.10a.

Fig.10c is an eye diagram illustrating the preferred placement of signals with reference to each other according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

In Fig.1a, an example embodiment of the present invention in its most
10 general way is illustrated. As shown in the figure, register 12 has a plurality of channels having inputs 2 and outputs 18, wherein one of the channels, D0 – DQ0, is used to deskew the register using a reference signal 11. Reference signal 11 in this example embodiment is preferably supplied by the reference generator 3 that generates the signals having wave forms shown in Fig.1b.

15 Typically, any media including transmission lines, clock networks, etc is frequency dependent. Different factors, such as RC networks, dielectric coefficient, reflections and standing waves, contribute to this dependence so that in the absence of special measures directed on elimination of these factors, they will inevitably increase the setup/hold time. Therefore, in the present invention, a
20 reference signal is provided, as described above, which seldom changes thereby allowing complete settlement, so that its history pattern would not affect the moment of reading data.

To achieve this, before the reference signal changes state, its value is maintained at the same logic value for a certain number of clock periods to allow
25 all reflections to dissipate so that to obtain a reference signal which is free of changes caused by previous transition as illustrated in Fig.1b.

The reference signal generator 3 provides also a Sample Enable signal which shall be active for not more than one period of clock signal during the cycle

following the referenced edge as shown in Fig.1b. In case of analogue feedback circuitry, the obtained Sample Enable signal is supplied to a Sample Hold device 13. In case of digital feedback circuitry, the obtained Sample Enable signal may be simply connected to Clock Enable input of the flip-flop connected to the output

5   of register 12. In this case, the flip-flop would provide the function of the Sample Hold Device 13 shown in Fig.1a.

Further, the system comprises a variable delay 8 which may be implemented as described in detail below. The output of the register is connected to detecting means 15 for determining a deviation from some predetermined level

10   of probability of reading a desired symbol by said register. The detecting means may be implemented in an integrator shown in Fig.2d and a low pass filter shown in Fig.2c, or as a phase comparator as shown in the embodiment of Fig.5. Other suitable means may be selected by a specialist in the art. The output of the detecting means 15 is fed to the delay 8, for example such as shown in Fig.2b,

15   which uses the determined information on deviation from the predetermined level of probability to generate a feedback signal to compensate timing errors in said register.

It may be explained in more detail with reference to Fig.7b, that the selection of a range of probability (shown as ΔP) shall be considered as an

20   important feature of the invention as it defines the accuracy of placement of the moment of reading data with respect to a reference (shown as Δt) and thus, the performance of the system in whole. In comparison, according to US 6,002,282, an integrator in Fig.4, obviously, can provide some reference that is defined by a threshold of element 216, however, this threshold itself depends on temperature

25   and supply voltage and therefore, would have an indefinite position on the curve of Fig.7b, e.g. within an interval ΔP_1 of probability giving the wide interval $\Delta \tau_1$ for a moment of reading data in respect to the reference, while the narrow predetermined level of probability shown by ΔP_2 would result in accurate placing of the moment of reading data within the range $\Delta \tau_2$ and thus, in accurate reading

30   of data.

A second example embodiment of the present invention is shown in Fig.2a. A self calibrating system according to this embodiment comprises a receiver implemented in register 12 which in this case has a degree of hysteresis, a low pass filter 14, integrator 16, a fixed delay 6, a variable delay 8 and
5 additionally a source 4 of modulator signal. Reference signal 11 generated by a reference signal generator 3 in this example embodiment is delayed by a fixed delay 6, preferably to centre the reference transition in the middle of the programmable range of the variable delay 8 on the clock path.

The output DQ0 of the reference channel D0-DQ0 from the register is
10 passed into a low pass filter 14, such as detailed in Fig.2c, then to an integrator 16 (a suitable integrator may be such as presented in Fig.2d, or some other integrator may be selected by a specialist in the art). The output of the integrator 16 is used to control an analog delay 8 with a monotonic transfer function such as detailed in Fig.2b, or a digital delay, such as MC 100E195 manufactured by
15 Motorola Inc. Let us assume that register 12 has a hysteresis, for example, due to input voltage hysteresis, bushold function or, timing hysteresis caused by setup time dependence on the register's output state.

In this case we can phase modulate the clock signal shown in Fig.4b by another signal, called modulator signal, which signal does not change the mean
20 value of the register 12 output, from the source 4 in mixer 10. In most cases this signal can be a saw tooth, a triangular wave, such as, for example, shown in Fig.4a, or even white noise to maintain the accuracy of the reference signal. The modulator signal imposes a phase, or other manipulation with a phase component of the clock signal, such as adding periodic signal on the clock
25 signal. For the clock and modulator signal shown in Figs. 4b and 4a, respectively, the resulting reference signal 11 will be as shown in Fig.4c.

It is appreciated that in the absence of the signal hysteresis, the circuitry as described in Fig.2a may be simplified by omitting the above described means for generating the modulator signal.

The means for generating a modulator signal according to the second example embodiment of the present invention may be implemented as described in detail with reference to Fig.3.

As shown in Fig.3, an advantageous method of generating and applying the modulator signal is to use another channel of the same register to produce a triangle signal formed by low pass filter 24, inverting integrator 26 and resistors 22 and 23, where feedback from a low pass filter or integrator connected to the output of that channel back to the input causes a triangular wave to be generated.

For a system as shown in Fig.3, the transfer function corresponding to the case when the feedback loop is opened, is presented in graph 2 of Fig.4f, which illustrates effect of hysteresis in register 12. While in the case of absence of hysteresis, the transfer function will be as shown in graph 1 of Fig.4f (in some cases the transfer function may be linear, in some cases not linear).

Thus, an additional objects of the present invention according to this embodiment is converting the system having a hysteresis into a hysteresis-free system.

This is required to obtain a stable behaviour of the above system and thus, to reduce the skew by a half width of the hysteresis loop. In this case, the signal at the output of the register 12 will have a randomly modulated pulse width as shown in Fig.4e, instead of random values of this output, as shown in Fig.4d. In both cases, when the system reaches the stable state, the mean value of the signal at the output of the filter 14 is equal to the half amplitude of the signal at the output of the register 12 that corresponds to the maximum level of phase noise where the probability to capture "1" and "0" is equal to each other, i.e. 50/50.

The ratio between resistors 22 and 23 determines the amplitude of the triangle modulating signal imposed on the reference being divided by the ratio between terminating resistor 21 and reference source impedance. Preferably, the

depth of modulation of the reference signal shall slightly exceed the hysteresis loop width that allows to calculate the optimal ratio for resistors 22, 23. A third example embodiment of the present invention illustrates how the problem of eliminating output channel skew may be solved with respect to a transmitter by

5 using the self calibration according to the present invention.

Fig.5 is a block diagram of a transmitter with expandable data width (i.e. with a great number of channels) which can be much higher than provided by a single register, in accordance with the third embodiment of the present invention wherein a phase comparator is used to maintain output zero skew between

10 multiple driving registers.

Different types of phase comparators may be used for deskewing the transmitter, for example, a flip-flop may be exploited. In this case, to one input of this flip-flop, which may be either a clock input, or data input, the reference signal is connected, while to the other input a sense signal is connected. Alternatively,

15 the phase comparator 20 can be made as a circuitry shown in Fig.1a, with the addition of integrator shown in Fig.2d.

It shall be evident for a specialist in the art that data transmitting lines of the register may be used as sense signals for the phase comparator, however, in this case, the comparator shall ignore cycles which do not have any transitions

20 that may be implemented by using signals on inputs of the register on a previous cycle.

It shall be noted that the important advantage of the proposed invention is that it allows to compensate and eliminate the skew "on the fly" during the operation.

25 A detailed example embodiment of the self calibrated transmitter is illustrated in Fig.6. In this embodiment the phase comparator is implemented in a receiver shown in Fig.2a. It is also appreciated that circuitry elements in this figure designated by the same position numbers as in Figs. 2a and 3 are the same as already described, or equivalents thereof.

In Fig.6, register 12 is an auxiliary register which serves to deskew transmitting register 30; both registers being connected in series, with the feedback circuit comprising low pass filters 32 and 14 feeding integrators 33 and 16, to generate feedback signals to deskew the outputs of register 30 and inputs

5   of register 12 to transmitter reference signal using verniers or analogue delay elements 8 and 37. The total skew in this situation amounts to a sum of intra-channel input skew of the auxiliary register 12 and intra-channel output skew of register 30. By the means described herein the overall timing inaccuracy of an entire system can be reduced to less than 10ps after compensation for the

10   differential track lengths between channels due to packaging.

Still another example embodiment of the self calibrated transmitter is illustrated in Fig.8. In this embodiment the phase comparators are also implemented in receivers shown in Fig.2a. It is also appreciated that circuitry elements in this figure designated by the same position numbers as in Figs. 2a, 3

15   and 6 are the same as already described, or equivalents thereof.

In Fig.9, registers 12, 52 are auxiliary registers for deskewing transmitting register 30. Register 52 is connected to the falling edge sense line of transmitter 30 to control the falling edge of the transmitter's output with respect to the reference clock and register 12 is connected to the rising edge sense line of the

20   transmitter to control the rising edge respectively.

The auxiliary self–calibrated receiver 52 serves for controlling falling edge and odd rising edge timings and comprises three feedback circuits.

The first feedback circuit serves for self-calibration of register 52 and includes a low pass filter 54 feeding integrator 56 for generating a feedback

25   signal using analogue delay element 37 similarly to as has been already described with reference to Fig.6.

The second feedback circuit serves for deskewing the odd rising edge of register 30 and includes low pass filter 53 feeding integrator 55 and duty cycle correction stage and frequency doubler 41.

The third feedback circuit includes low pass filter 35 feeding integrator 36 and serves for controlling the transmitter's 30 power supply voltage (V) and balance the threshold transition points (. corresponding, e.g. to high and low power supply voltages as explained in Fig.8b.

The auxiliary self-calibrated receiver 12 serves for controlling even rising edge timings and comprises two feedback circuits, the first being for self-calibration of register 12 and includes a low pass filter 14 feeding integrator 16 for generating a feedback signal using analogue delay element 8, and the second for generating a rising edge feedback signal to deskew the even rising edge of the output of register 30 with respect to transmitter reference signal using verniers or analogue delay elements 37.

The total skew in this situation amounts to a sum of intra-channel input skew of the auxiliary registers 12 and 52 and intra-channel output skew of register 30. By the means described herein the overall timing inaccuracy of an entire system can be reduced to few picoseconds after compensation for the differential track lengths between channels due to packaging.

Operation

The operation of the invention will now be illustrated with respect to the example embodiment shown in Fig.2a.

On power up, assume the variable delay 8 is at minimum. This means the system will have a maximum negative skew. In this situation, the clock obeys all setup requirements for the reference line and register 12 will be stable, that is it will not be in its timing uncertainty region of operation. Assuming inverting feedback, the register will produce a steady binary 1 on its output, which after the low pass filter 14 and integrator 16 causes a rising voltage on the output of the integrator, i.e. on the input to the clock vernier 8. This will cause the clock vernier 8 to increase in its delay value until the clock reaches a zero skew with respect to the reference signal after taking into account all setup and hold requirements caused by a difference between the propagation delay in the clock and data

paths within the register.

This will produce a stable level of the feedback signal, whether digital or analogue, matching the level which is the maximum level of timing uncertainty within the register, which corresponds to the predetermined level of probability, that is, with 50% of the output being a binary 1 and 50% being a binary 0. The above described operation may be also applicable to the example embodiment of Fig.3 as it shall be evident for a specialist in the art. In the embodiment of Fig.3 the modulator signal is generated by using another channel of the same register to produce a triangle signal formed by low pass filter 24, inverting integrator 26 and resistors 22 and 23.

In the case where the register has a degree of hysteresis, the modulator signal will push the reference signal in and out of the timing uncertainty region on each side (as illustrated in Figs.4a-4f). This will produce signal which will vary from continuous binary 0s on the corresponding output channel of the register, to continuous binary 1s, with the phase noise state framed equally by these two stable states, such that if the output of the register was sampled then the number of 1s and 0s appearing would be equal.

The operation of the third example embodiment shown in Fig.6 will now be described. It shall be appreciated that the circuitry including elements 8, 12, 14, 16, operates in the same mode as described with reference to Figs.2-3, so that register 12 has a zero input skew in relation to transmitter reference signal.

In the third embodiment, after register has reached a stable position at a predetermined level of probability of reading a desired symbol in a sequence of symbols, e.g. at the maximum of its phase noise in the channel D0-DQ0, assume the variable delays 8, 37 are at minimum. This means the transmitter 30 has a maximum negative skew. In this situation, the signal from the output DQ0 of transmitter 30 obeys all setup requirements for the input D1 of auxiliary receiver 12 and channel D1-DQ1 is also in its stable state.

Assuming inverting feedback, the channel D1-DQ1 of register 12 will

produce a steady binary 1 on its output DQ1, which after the low pass filter 32 and integrator 33 causes a rising voltage on the output of the integrator 33, i.e. on the input to the clock vernier 37. This will cause the clock vernier 37 to increase in its delay value until matching the level of probability which

5   corresponds to the maximum level of phase noise within the channel D1-DQ1 of register 12, that is with 50% of the output DQ1 of register 12 being a binary 1 and 50% being a binary 0, i.e. the sense signal from channel DQ0 of the transmitter 30 reaches a zero skew with respect to the transmitter reference assuming the skew on the input D0 of register 12 in relation to transmitter reference is already

10   zero.

Thus, the maximal skew between the output DQ0 of register 30 and transmitter reference will be determined by the input intra-channel skew of the auxiliary register 12. Thus, outputs DQ1-DQN of transmitter 30 will have a skew with respect to transmitter reference which is not more than the sum of intra-

15   channel output skew of transmitter 30 and intra-channel input skew of register 12.

The operation of the forth example embodiment shown in Fig.9 will now be described in detail. It shall be appreciated that the even rising edge deskewing circuitry incorporating elements 8, 12, 14, 16, 30, 32, 33, 37 operates in the same mode as described with reference to Figs.2a ,3 and 6.

20   According to the forth embodiment, to provide the symmetry of the rising and falling edges, the following procedure is performed.

First, the position of the falling edge is determined with respect to the reference clock. When the falling edge crosses the threshold line earlier than the reference clock, it means that the power supply voltage is low. In this case, an

25   error signal produced by the phase comparator 52 passes through low pass filter 35 and causes integrator 36 to increase its output voltage which is supplied into the transmitter 30 so that the transmitter's power supply voltage also rises.

It shall be also appreciated that the above correction procedure may be implemented using parameters influencing the symmetry of the falling and rising

edges, other than power supply voltage, for example, slew rate control, or others, as is evident for a specialist in the art.

Each step of the correction moves the transition point to the right until it coincides with the reference clock and the error signal at the output of the phase comparator 52 corresponds to the maximum of timing uncertainty as has been described in detail above.

To exclude the duty cycle irregularities, the procedure is performed as follows.

As far as a DDR system transmits two bits of information per each clock period, a driver (transmitter) is required which is capable of changing its state accurately on each edge of the main clock, i.e. a "DDR" type clock is needed. In Fig. 8c a block scheme is shown illustrating a clock doubler which forms two rising edges per each clock cycle out of the falling and rising edges of an input clock signal.

However, in this circumstances, an additional source of inaccuracy arises in connection with the possible inequity of times of high level and low level states of input clock signal and other inaccuracies caused by clock doubler or, for example, transmitter. For the purposes of the present explanation, even data transmission slot corresponds to rising edge of input clock, wherein odd data transmission slot corresponds to falling edge of input clock.

Assuming, at the beginning, that the time intervals between toggles at transmitter's outputs driving sense lines corresponding to the rising and falling edges of transmitter's reference are not equal, as shown in Fig.9, wherein the odd rising edge appears before the transmitter's reference that corresponds to the high voltage level of threshold input on duty cycle correction stage incorporated in unit 41.

In this case, an error signal produced by the phase comparator 52 passes through low pass filter 53 and causes integrator 55 to decrease its output voltage. As a result, the duty cycle of the clock signal at the output of the duty cycle

correction stage incorporated in unit 41 shown in Fig.9 increases. Thus, the odd rising edge is being delayed until it matches the transmitter's reference.

Thus, odd rising edges are also placed exactly in the position of the transmitter's reference edges. Being reminded that even rising edges are simultaneously deskewed as has been described above, the skew caused by rising and falling edge asymmetry is practically eliminated.

To provide the maximum channel bandwidth, or the highest possible data rate with a predefined bit error rate (BER), the following technique is proposed as illustrated in Figs.10a and 10b. Typically, BER is in a range from 10^{-3} to 10^{-15} depending on a particular application requirements.

The system illustrated in Fig.10a comprises a driver 61, a receiver 62 and a generator 63 for generating reference signals for driver 61 and receiver 62. The reference signal generator generates signals as shown in Fig.10b.

Let us consider Fig.10c illustrating a channel of data transferred through a media. As has already been discussed in detail above, the probability of reading a symbol an a sequence of symbols in a channel can be described by a probability curve from Fig.7b. Using this curve, it is possible to define the amount of time for which a moment of reading data shall be ahead of the driver's reference where the probability corresponds to a predefined level, e.g. 50/50 to correspond to the required BER.

To achieve this, it is necessary to find a point on the curve having a height of the required BER. The time difference between the time "0" and the time determined by this point will be Δ. Now, it is obvious that the Receiver reference shall differ from the Driver reference by this amount of time Δ as shown in Fig.10b. Therefore, after Δ is defined, it is possible to maintain the predefined BER level and maximum data rate, if symbols are transmitted through a channel with a rate of 2Δ per one symbol as illustrated in Fig.10c.

It shall be mentioned that all the above described feedback loops shall present the negative feedback to provide a stable operation and may require

using additional circuitry elements as is evident for a specialist in the art.

It shall be appreciated also that other embodiments and modifications of the present invention are possible within the scope of the present invention. Thus, the invention may be applied to compensating skews in communication systems that can serve to increase the bandwidth of signal transmission. Also, it can be used to reduce the distribution of the phase noise and its effect on changes in the clock to output delays or changes in the actual setup and hold time. It can be applied to reduce timing dispersion of a signal in cases when signals are transmitted via an optical cable or via the ether and in various other applications including application specific integrated circuits (ASIC) comprising digital interfaces requiring low skew.